REMARKS

Claims 43-107 are pending.

Claims 43-66, 98, 103,106 and 107 were constructively elected while claims 67-97, 99-102, 104 and 105 were deemed withdrawn from consideration as being directed to a non-elected invention (species). Applicant does not traverse the restriction requirement with respect to claims 67-97, 104 and 105 and cancels same in this amendment. Applicant provisionally elects with traverse to continue prosecution of the constructively elected claims 43-66, 98-103, 106 and 107. In making this election, applicant reserves the right to file one or more divisional or continuation applications directed to subject matter of the canceled claims.

In traverse, applicant respectfully requests reconsideration of the restriction requirement in regard to dependent claims 99-102, given that they depend from elected generic independent claim 98 and are themselves generic. If the independent claim 98 is allowed, then dependent claims 99-102 would also be allowable at least by reason of being dependent upon an allowable generic claim.

Claims 43-66, 98-103, 106 and 107 remain in this case for reconsideration.

The Rejections Under §112, Second Paragraph:

Claims 45, 51, 52, 55, 56, 65 and 66 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant respectfully traverses, and submits that the claims are sufficiently definite to point out and distinctly claim the subject matter of the invention. Nonetheless, to advance this case to allowance, a few changes have been made.

In dependent claim 45, which is dependent on claim 44, the "the insulative layer" at line 2 would be understood to refer to "insulating layer" as set forth in line 3 of claim 44. Applicant has replaced "insulative" with "insulating".

With reference to claim 51, which is dependent upon claim 50, claim 50 has been amended to define at least one vertically-oriented sidewall spacer extending upward from the upper surface of the substrate, with the at least one vertically-oriented sidewall spacers atop

respective vertically-oriented layers. Further, in claim 51, "one" has been replaced with "at least first and second", and the phrase "each side" replaced with "respective sides".

Regarding claim 52, the "sidewall spacers" has been replaced with "vertically-oriented sidewall spacers."

Regarding claim 55, at line 4, "said plurality" has been replaced with "said plurality of islands". Similarly, for claim 56 at line 5, "said plurality" has been replaced with "said plurality of fingers."

Each of claims 65 and 66 has been amended to depend from claim 44 and to incorporate the features of claim 60.

Accordingly, applicant submits that the claims now meet the requirements of §112, second paragraph.

The Rejection Under 35 USC §112, First Paragraph:

Claims 43-66, 98, 103, 106 and 107 stand rejected under 35 USC §112, first paragraph, for having subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant respectfully traverses, and submits that the subject matter of these pending claims are adequately described to convey possession of the claimed invention to those skilled in the art.

Certain details of exemplary embodiments of the present invention are disclosed in greater particularity in parent applications within the lineage of this case, which parent applications (i.e., U.S. Pat. Nos. 4,895,810 and 5,262,336) were incorporated by reference at page 9, lines 15-17 and page 14, lines 13-14. Considering some of these details repetitive of that already set forth in the prior applications, applicant chose to incorporate some of this information through use of the incorporation-by-reference procedures.

not related to the claimed subject matter

The Manual of Patent Examining Procedures, i.e., MPEP 608.01(p), provides guidance for incorporation by reference, as excerpted below for the convenience of the Examiner.

> The Commissioner has considerable discretion in determining what may or may not be incorporated by reference in a patent application. *General Electric Co. v. Brenner*, 407 F.2d 1258, 159 USPQ 335 (D.C. Cir. 1968). The incorporation by reference practice with respect to applications which issue as U.S. patents provides the public with a patent disclosure which minimizes the public's burden to search for and obtain copies of documents incorporated by reference which may not be readily available. Through the Office's

> incorporation by reference policy, the Office ensures that reasonably complete disclosures are published as U.S. patents.
>
> * * *
>
> An application as filed must be complete in itself in order to comply with 35 U.S.C. 112. Material nevertheless may be incorporated by reference, *Ex parte Schwarze*, 151 USPQ 426 (Bd. App. 1966). An application for a patent when filed may incorporate "essential material" by reference to (1) a U.S. patent, (2) a U.S. patent application publication, or (3) a pending U.S. application, subject to the conditions set forth below.
>
> "Essential material" is defined as that which is necessary to (1) describe the claimed invention, (2) provide an enabling disclosure of the claimed invention, or (3) describe the best mode (35 U.S.C. 112). In any application which is to issue as a U.S. patent, essential material may not be incorporated by reference to (1) patents or applications published by foreign countries or a regional patent office, (2) non-patent publications, (3) a U.S. patent or application which itself incorporates "essential material" by reference, or (4) a foreign application. MPEP 608.01(p).

Nonetheless, applicant has submitted herewith, certain amendments to the specification of the present application. These amendments copy portions of the prior incorporated applications and, therefore, do not introduce new matter. The MPEP addresses amendments to an application which are supported in the original description, as follows:

> 2163.07(b) Incorporation by Reference
> Instead of repeating some information contained in another document, an application may attempt to incorporate the content of another document or part thereof by reference to the document in the text of the specification. The information incorporated is as much a part of the application as filed as if the text was repeated in the application, and should be treated as part of the text of the application as filed. Replacing the identified material incorporated by reference with the actual text is not new matter. MPEP §2163.07(b).

Additionally, for amendments that address functions or properties inherent to, e.g., a device previously disclosed, the MPEP states:

> 2163.07(a) Inherent Function, Theory, or Advantage
> By disclosing in a patent application a device that inherently performs a function or has a property, operates according to a theory or has an advantage, a patent application necessarily discloses that function, theory or advantage, even though it says nothing explicit concerning it. The application may later be amended to recite the function, theory or advantage without introducing prohibited new matter. *In re Reynolds*, 443 F.2d 384, 170 USPQ 94 (CCPA 1971); *In re Smythe*, 480 F. 2d 1376, 178 USPQ 279 (CCPA 1973). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted). MPEP §2163.07(a).

Claim 43 defines "a gate metal layer coextending over the doped polysilicon." Applicant submits that such features are supported by the specification of the present application, which includes incorporated U.S. Pat. No. 4,895,810, column 12, lines 25-64. Additionally, the "co-extending" property of the metal has been brought within the language of the present specification as supported by the application – e.g., including, but not limited to (i) the inherent properties of the metal or silicide depositions, (ii) FIG. 6B from incorporated U.S. Pat. No. 4,895,810 and (iii) incorporated U.S. Pat. No. 4,895,810, at column 12, lines 25-64, portions of which are now more expressly recited within the text of present application.

Claim 44 defines "an insulating layer over the gate conductor; and an upper metal layer over the insulating layer and contacting the gate conductor through a via in the insulating layer." Applicant submits that the specification of the present application, which includes incorporated U.S. Pat. Nos. 4,895,810 and 5,262,336, supports such features. The present specification at page 14, lines 25-27, describes that the completion steps "include opening gate contact vias at discrete locations . . . and passivating the surface." Additionally, the provision of "upper metal and insulating layer" are supported within the application – e.g., including, but not limited to incorporated U.S. Pat. No. 5,262,336, at column 15, lines 31-54. The present application has been amended to expressly recite some of this incorporated material within the text of the specification. Applicant further submits that the upper metal inherently contacts the gate metal through the insulative layer through at least some type of via or opening, e.g., including the disclosed opened-gate contact vias of the passivated surfaces, as persons skilled in the art would know.

not OK

no such metal layer, insulating layer and the via in the patents

Likewise, claim 45 defines "a portion of the upper metal layer over the insulative layer contacting the source conductor in electrical isolation from the gate conductor." Applicant submits that the specification of the present application, which includes incorporated U.S. Pat. Nos. 4,895,810 and 5,262,336, supports such features, such as forming insulating material over the source. As set forth in the present application, the insulating material can comprise the insulating material 272, such as that of FIG. 6C and/or other insulating or passivation material as incorporated by reference from U.S. Pat. No. 5,262,336. Regarding the upper metal over the insulating material, such structure also is supported by the application – e.g., including, but not limited to incorporated U.S. Pat. No. 5,262,336, at column 15, lines 31-54. The present application has been amended to expressly recite at least some of such exemplary incorporated subject matter within the text of the specification.

not OK

gate pad and gate bus only, no gate wiring connected to the source electrode

Finally, applicant further submits that such upper metal is inherently understood to contact the source conductor (through the insulating material) by way of at least some well-known provision, e.g., such as a via.

Claim 46 defines "an insulating layer over the gate conductor; and an upper metal layer over the insulating layer and contacting the vertically-extending source conductor through a via in the insulating layer. For reasons similar to those presented above relative to claim 45, applicant submits that the specification of the present application supports such features of claim 46 – e.g., including by way of incorporated U.S. Pat. Nos. 4,895,810 and 5,262,336.

Regarding claims 60-65, applicant further extends the general traverse of the Examiner's rejection under §112, first paragraph, and additionally, again notes the support within the present specification as pointed out above relative to claims 43-46.

Concerning the insulating materials, and specific exemplary types, applicant submits that the specification supports such features – e.g., as set forth in incorporated 5,262,336. In addition, the specification of the present application has been amended to recite some of the exemplary insulating materials of incorporated-by-reference U.S. Pat. No. 5,262,336.

Claim 98 defines a gate structure comprising "metal disposed coextensively over the doped polysilicon" and that metallization contacts the gate structure through the insulating layer. Further, claim 103 further defines the metallization over the insulating material as comprising aluminum. Applicant submits that the present specification supports these features of claims 98 and 103 – e.g., similarly as submitted above relative to claims 43-46. Claims 99-102 are similarly supported.

Accordingly, applicant submits that the present application provides sufficient description to convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The Rejections Under 35 USC §103:

Claims 43-48, 50-53, 57, 58, 60-66, 98, 103 and 106 stand rejected under 35 U.S.C. §103 as being unpatentable over Sakamoto in view of Korman et al. Applicant respectfully traverses this rejection.

Independent claim 43 defines a

43. A recessed gate field effect power MOS device having a vertically-oriented channel comprising:

a semiconductor substrate including first and second laterally-extending layers of first and second opposite polarity dopants defining a body layer and an underlying drain layer;

a first trench having sidewalls extending depthwise from an upper surface of the substrate at least through the body layer to a bottom wall at a predetermined depth from the upper surface of the substrate;

a gate oxide layer on the trench sidewalls and the bottom wall of the first trench;

a gate conductor disposed within the first trench to a depth of at least an elevation of the upper surface of the substrate;

a vertically-oriented layer of semiconductor material extending upwardly along the gate oxide layer on the side thereof opposite the first trench, the vertically-oriented layer extending from the body layer to the upper surface of the substrate, the vertically-oriented layer comprising a first vertical layer portion contiguous with the body layer doped with said first polarity dopant to define an active body region including a vertical channel, and a second vertical layer portion atop the first vertical layer portion and forming a PN junction therewith, the second vertical layer portion being doped with said second polarity dopant to form a source region contacting the active body region; and

a vertically-extending source conductor contacting the vertically-oriented layer on a side thereof opposite the gate oxide layer and gate conductor, the source conductor electrically shorting the source region to the active body region across the PN junction;

the gate conductor comprising doped polysilicon contacting the gate oxide layer within the trench and a gate metal layer coextending over the doped polysilicon.

Sakamoto teaches of a vertical power MOSFET having a gate trench in a substrate having an oxide lining (FIG. 5(a)). Sakamoto further discloses disposing one of tungsten or polysilicon in the trench for the gate electrode.

Korman discloses a lateral power field effect semiconductor device having a body region self-aligned with respect to an aperture in the gate electrode. Korman teaches the gate electrode comprising titanium silicide disposed on polycrystalline silicon (FIG. 2N, column 8, lines 35-36).

As indicated by the Federal Circuit, a teaching or suggestion to make the claimed combination must be found in the prior art and not based on the Applicant's disclosure. *In re Vaeck*, 20 U.S.P.Q. 2d 1438 (Fed. Cir. 1991). Sakamoto does not disclose or suggest a need to improve its gate structure, nor looking to the teachings of Korman associated with dopant-self-aligning polysilicon-finger gates. Likewise, Korman does not disclose or suggest vertical power MOSFET devices of Sakamoto, assisting such vertical devices, nor that its dopant-self-aligning lateral gate-fingers could assist such vertical devices. Indeed, this is apparent per the teachings of Sakamoto for gates of vertical power MOSFETS that comprise either tungsten or polysilicon, not both. Based on these attributes, applicant submits that an artisan, upon reading these references, would not be motivated to combine teachings of the two references together nor to provide the particular combination of features as defined in the presently claimed invention. Rather, applicant respectfully proposes that the only suggestion

of a combination of Sakamoto and Korman comes from an impermissible hindsight reconstruction of the present invention. Accordingly, applicant submits that independent claim 43 is patentable over these references. Likewise, it follows that dependent claims 44-66 also are patentable, at least by reason of depending upon a patentable base claim.

Dependent claim 44 further defines an insulating layer over the gate conductor and an upper metal layer over the insulating layer and contacting the gate conductor through a via in the insulating layer. Because neither Sakamoto nor Korman disclose or suggest such features as defined in claim 44, applicant submits that a combination thereof also fails to provide such features and that, therefore, dependent claim 44 is patentable over Sakamoto and Korman either alone or in combination, independent of the patentability of its base claim.

Dependent claim 46 further defines an insulating layer over the gate conductor and an upper metal layer over the insulating layer and contacting the vertically-extending source conductor through a via in the insulating layer. For reasons similar to those presented in favor of the patentability of claim 44, applicant submits that claim 46 is patentable over Sakamoto and Korman either alone or in combination, independent of the patentability of its base claim.

Dependent claims 60 and 64 each define the gate metal layer as comprising aluminum. Again, Sakamoto teaches of a vertical power MOSFET having a gate trench filled with one of tungsten or polysilicon. Korman teaches of a gate electrode comprising titanium silicide disposed on polysilicon. Neither discloses aluminum on polysilicon for a gate structure as presently defined. Accordingly, applicant submits that dependent claims 60 and 64 are patentable over Sakamoto and Korman either singularly or taken together, independently of their base claims.

Additionally, dependent claim 62 further defines the gate conductor comprising refractory metal silicide over the polysilicon and beneath a gate metal, and 64 further defines the gate metal as comprising aluminum. Finding no disclosure or suggestion in Sakamoto and Korman for such multilayered gate conductors as defined in claims 62 and 64, applicant submits that dependent claims 62 and 64 are further patentable over these references independently of their base claims.

Claims 49 and 59 were rejected under 35 U.S.C. §103 as being unpatentable over Sakamoto in view of Korman et all, and further in view of Davis. Applicant respectfully traverses this rejection.

Dependent claims 49 and 54, further define that the first vertical layer portion contiguous with the body layer is doped to a first doping concentration and a laterally-extending portion of the body layer subjacent the first vertical layer portion has at least a top portion doped to a second doping concentration greater than the first doping concentration.

Davis discloses a MOSFET device comprising gate polysilicon (13), referencing FIG. 1 thereof, over gate oxide (12) over a lateral channel region in body material (20).

Davis does not show a vertical arrangement of first and second vertical layer portions of a recessed gate field effect power MOS device having a vertically-oriented channel as defined in claims 49 and 54. Indeed, applicant submits that an artisan upon reading Davis, would consider Davis to teach a lateral-channel device. Further, applicant respectfully notes an absence of some objective teaching in the prior art or knowledge generally available to one of ordinary skill in the art that would lead such individual to combine the relevant teachings of the references in a manner of that being claimed. Accordingly, applicant submits that there is no disclosure or suggestion of providing a combination of Davis and the other mentioned references, let alone, for providing the combination of features as presently defined in claims 49 and 54, and that, therefore, these claims are patentable.

Claims 55, 56, 59 and 107 were rejected under 35 U.S.C. §103 as being unpatentable over Sakamoto in view of Korman et all, and further in view of Blanchard. Applicant respectfully traverses this rejection.

Dependent claims 55, 56 and 107, further define that trench and the gate oxide layer and gate conductor within the trench form a gate structure which is laterally patterned in two dimensions to define an interconnected matrix enclosing a plurality of islands, or, alternatively, fingers of an interdigitated source-gate structure.

Blanchard teaches a process for making a DMOS, including lining a groove with a dielectric material to form an inner groove having sidewalls, and lining the inner groove with a dielectric material to obtain increased thickness of the gate dielectric on the sidewalls of the inner groove. Referencing FIGS. 4h and 4i, Blanchard further teaches of polysilicon material (33) in the groove.

Applicant submits that Blanchard lends nothing further to the disclosures of Sakomoto, Korman and Davis, that has not already been addressed above, disclosing or suggesting the combination of features of the presently claimed invention. Therefore, dependent claims 55, 56, 59 and 107 are patentable over Sakomoto, Korman and Blanchard,

either singularly or taken together, for reasons corresponding to those previously advanced herein.

Regarding independent claim 98, applicant respectfully notes that support for this claim can be traced back to applicant's U.S. Pat. No. 4,895,810, which has priority as early as May 17, 1988. Sakamoto, Korman, Davis and Blanchard post-date this priority and, therefore, are not available as prior art relative to independent claim 98. Accordingly, claim 98 is patentable over these references together with dependent claims 99-103, 106 and 107.

the last two paragraphs of claim 98 are not supported by the spec. of 4895810

In view of the above amendments and remarks, applicants urge the allowance of claims 43-66, 98-103,106 and 107, and respectfully request such action for this case.

If any questions remain, the Examiner is requested to call the undersigned.

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PATENT TRADEMARK OFFICE

Respectfully submitted,
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the specification:

On page 12, before line 4, the following paragraphs have been inserted:

-- U.S. Pat. No. 4,895,810, incorporated by reference herein, teaches exemplary metal processes to reduce resistance across a surface of the gate polysilicon between the two sidewall spacers. Referencing FIGS. 6B (FIG. 19 of U.S. Pat. No. 4,895,810), a metal layer of substantial electrical conductivity, preferably 500 to 1,000 angstroms of tungsten, is deposited by selective CVD deposition to form ohmic contacts 275, 276 in silicon trench 263 and on the polysilicon layer 232. This means of tungsten deposition preferentially metallizes the exposed silicon (new layer 275) and polysilicon (new layer 276) surface but not the oxide sidewalls 262a. Alternatively, contacts 275, 276 can be made by selective silicide formation.

To carry the high current out of the silicon, additional metal has to be placed on top of the tungsten layer. This may be done by many methods including plating, evaporation and sputtering. If plating is utilized, and/or lead based plating, the new metal layer plates out preferentially on tungsten requiring no metal etching afterwards. If sputtering or evaporation of aluminum is used, more steps are needed since these deposition techniques are typically not sufficiently selective.

As shown in FIG. 6B, as inherently effected by the selective depositions, the metal and/or silicide are formed co-extensively over the polysilicon surface. --

On page 14, after line 28, the following paragraphs have been inserted:

-- Further to such completion and as incorporated herein by reference to U.S. Pat. No. 5,262,336, for example, a second layer of metal is deposited in gate pad regions of the gate contact layer in isolation from the source pads over a passivation layer. Additionally, a double or a triple layer of metal can be deposited in the source bonding pad and bus areas. This measure improves current handling capability, links the source metal areas together in isolation from the gate pads and busses.

Referencing FIGS. 6C (FIG. 16B of U.S. Pat. No. 5,262,336), a layer 272 can be applied on top of areas 230 and 228. This layer may be a resin such as photoresist or any number of other compounds such as polyimide or spin-on glass. Layer 272 is applied to assist surface planarization and may be applied using spin, spray, or roll-on techniques familiar to

one skilled in the art to give the preferred coating. Planarization can be done by conventional techniques familiar to one skilled in the art, such as plasma etching, ion milling, reactive ion etching, or wet chemical etching. The underlying layers 228 and 230, of the source and gate respectively, remain covered and thus unetched. Next, artifacts 274 are etched away, and any metal extending downward along the sidewalls can be removed by continuing the etch. In some procedures, layer 272 is then removed by any conventional means. However, if layer 272 is a material that can remain on the device surface, such as glass, its removal is not necessary. A passivation layer is then deposited, as is commonly done.

In accordance with an exemplary embodiment of the present invention, the passivation layer comprises at least one of the group consisting of oxide, nitride, glass and phosphosilicate glass (PSG), e.g., as set forth in incorporated 5,262,336 (e.g., at column 24, line 61 to column 27, line 50). --

In the drawings:

New Figs. 6B and 6C are added.

In the claims:

Claims 45, 50-52, 55-56 and 65-66 have been amended as follows:

45. (Amended) A recessed gate field effect power MOS device according to claim 44 wherein a portion of the upper metal layer over the [insulative] insulating layer contacts the source conductor in electrical isolation from the gate conductor.

50. (Amended) A recessed gate field effect power MOS device according to claim 43 including [a] at least one vertically-oriented sidewall spacer extending upward from the upper surface of the substrate, the at least one vertically-oriented sidewall spacers atop [the] their respective vertically-oriented layers.

51. (Amended) A recessed gate field effect power MOS device according to claim 50 including [one] at least first and second of said vertically-oriented layer on [each side] respective sides of the trench, each having one of said vertically-oriented sidewall spacer

thereon, and an insulative layer extending laterally between the sidewall spacers over the gate conductor.

52. (Amended) A recessed gate field effect power MOS device according to claim 51 including an upper metal layer extending over the insulative layer and the vertically-oriented sidewall spacers and contacting the vertically-extending source conductor.

55. (Amended) A recessed gate field effect power MOS device according to claim 43 in which the first trench and the gate oxide layer and gate conductor within the trench form a gate structure which is laterally patterned in two dimensions to define an interconnected matrix enclosing a plurality of islands, each of said plurality of islands containing a downward extending finger of source conductor surrounded by a portion of the active body region including said vertical channel, the channel having a width defined in each island by a perimetral length of the island.

56. (Amended) A recessed gate field effect power MOS device according to claim 43 wherein the first trench, the gate oxide layer and the gate conductor together form a gate structure configured as a finger, said recessed gate field effect power MOS device comprising a plurality of said finger;

the source conductor intermediate the fingers of said plurality of fingers to define an [interdigited] interdigitated source-gate structure.

65. (Amended) A recessed gate field effect power MOS device according to claim [60] 44, wherein the gate metal layer comprises aluminum, and the upper metal layer comprises aluminum.

66. (Amended) A recessed gate field effect power MOS device according to claim [60] 44, wherein the gate metal layer comprises aluminum, and the insulating layer comprises at least one of the group consisting of oxide, nitride, oxy-nitride, glass, and phosphosilicate glass (PSG).

Claims 67-97, 104 and 105 have been canceled.

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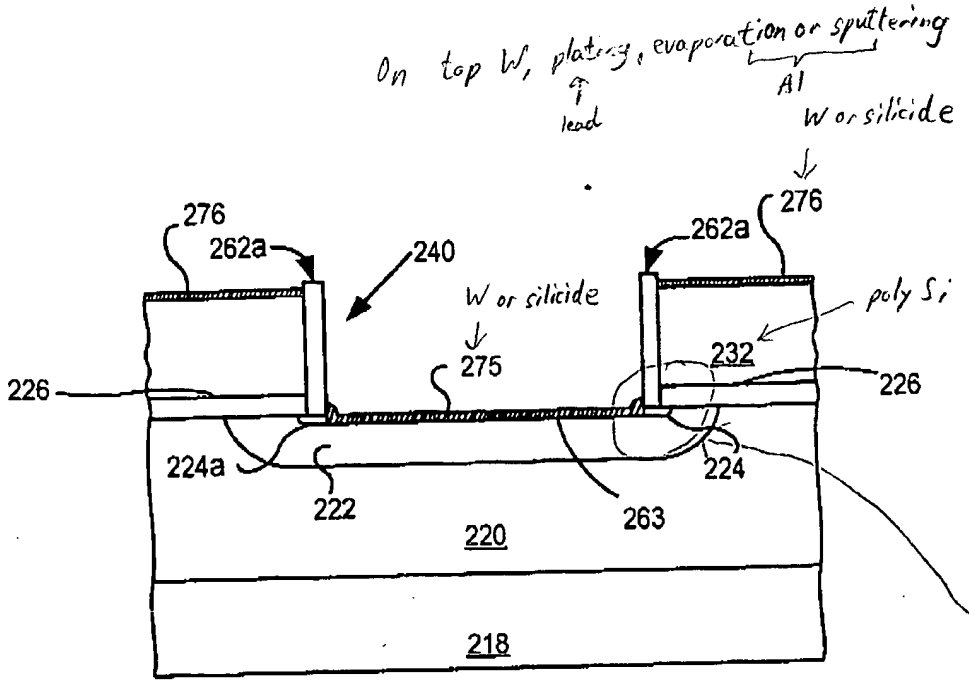

FIG. 6B

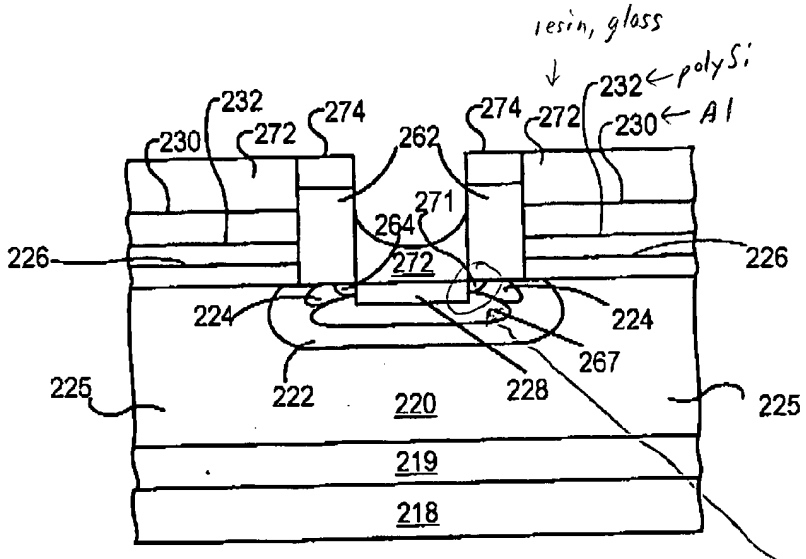

FIG. 6C